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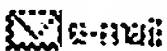
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1. **An adaptive CMOS transmission line driver**

Patel, H.N.; Hohl, J.H.; Oalusinski, O.A.;  
ASIC Conference and Exhibit, 1993. Proceedings., Sixth Annual IEEE International  
27 Sept.-1 Oct. 1993 Page(s):460 - 463

[AbstractPlus](#) | [Full Text: PDF\(240 KB\)](#) IEEE CNF

IEEE STD IEEE Standard



2. **Optimum repeater insertion based on a CMOS delay model for on-chip RLC inter**

Ismail, Y.I.; Friedman, E.G.;  
ASIC Conference 1998. Proceedings. Eleventh Annual IEEE International  
13-16 Sept. 1998 Page(s):369 - 373

[AbstractPlus](#) | [Full Text: PDF\(556 KB\)](#) IEEE CNF



3. **Embedded at-speed test probe**

Aigner, M.;  
Test Conference, 1997. Proceedings., International  
1-6 Nov. 1997 Page(s):932 - 937

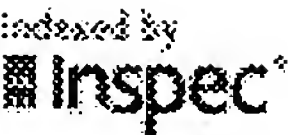
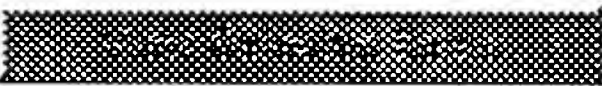
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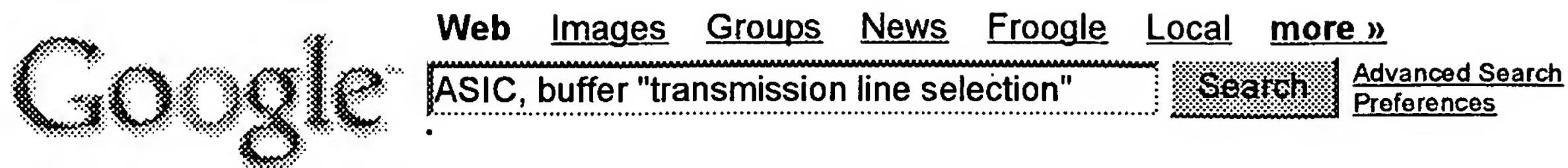


4. **Package clock distribution design optimization for high-speed and low-power VL**

Qing Zhu; Tam, S.;  
Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging  
Transactions on [see also Components, Hybrids, and Manufacturing Technology, IEEE  
Volume 20, Issue 1, Feb. 1997 Page(s):56 - 63

[AbstractPlus](#) | [References](#) | [Full Text: PDF\(228 KB\)](#) IEEE JNL





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